Proceedings of 10th International Conference on Precision, Meso, Micro and Nano Engineering (COPEN 10)
December 07 – 09, 2017, Indian Institute of Technology Madras, Chennai – 600 036 INDIA

Formation of Voids in Cu-Sn Metal Stacks for MEMS Applications

Harindra Kumar Kannojia* **and Pradeep Dixit**

Department of Mechanical Engineering
Indian Institute of Technology, Mumbai – 400076, INDIA

Abstract

Solid-liquid interdiffusion (SLID) bonding depends upon rapid growth of intermetallics (IMCs) between a high melting point and a low melting point metals. Cu-Sn SLID bonding has gained interest due to its inherent advantages of low processing temperature and less stringent surface uniformity requirements. But at the same time, reliability of SLID assisted hermetic packaging and interconnections greatly depends upon intermittent voids developed in different levels of the bond, since they reduce the effective contact area. These voids can occur due to various processing parameters like electroplated metal quality, annealing temperature, time and even due to the difference in diffusion rates of two metals involved, commonly referred to as kirkendall effect. In this paper, the void formation and growth in Cu-Sn metal stacks annealed at 250 °C, 275 °C and 300 °C for 10, 60 and 150 minutes are presented. Number of voids, void density per unit length and void area at different locations are calculated using image processing software.The annealed Cu-Sn metal stacks show uniform layer of Cu_3Sn intermetallic compound (IMC) with irregularly distributed voids into the IMC and Cu-Cu_3Sn interface. It is observed that at given annealing temperature, void size increases and void fraction decreases as a function of increasing annealing time. Voids are observed to be least in bond pads annealed at 275 °C.

Keywords: Voids, MEMS, Hermetic Encapsulation, Solid-Liquid Interdiffusion Bonding, SLID, IMCs, 3-D Packaging.

1. INTRODUCTION

Micro-Electro-Mechanical-Systems (MEMS) devices often include moving structural elements which in turn requires controlled environment in their vicinity to inhibit damping effects and increase product's reliability. This can be achieved by hermetic packaging of MEMS devices to achieve better performance and long term reliability. As per the commercialization aspect, cost is a very critical parameter and MEMS packaging, constitutes a major part of total device's cost [1]. Thus, there is an urgent need of low cost, mechanically robust, highly reliable and hermetic packaging solutions.

Different bonding techniques are being used in MEMS technology like fusion bonding, anodic bonding, eutectic bonding, thermo-compression bonding, etc. These bonding techniques possess some critical drawbacks like high processing temperatures and extreme surface uniformity requirements. Since, MEMS requires low processing temperatures due to the presence of low melting point metals (e.g. Al) and in addition has not so good surface uniformity due to the deposition process employed (e.g. electrodeposition), there has been a strong need for such a process which can circumvent these stringent requirements. The Solid-liquid interdiffusion bonding (SLID) is a bonding technique which has low processing temperatures and minimal surface requirements. SLID bonding can also be used to form interconnections simultaneously with hermetic packaging, since the intermetallic compounds (IMCs) formed are electrically conductive [2]. Thus SLID bonding technique can be utilized to attain hermetic encapsulation with simultaneous fabrication of interconnections, resulting in efficient fabrication process with reduced manufacturing cost and time. SLID bonding technique relies on rapid formation of IMCs between a high melting point ($T_{m,\ high}$) metal (e.g. Au, Cu, Ni) and a low melting point ($T_{m,\ low}$) metal (e.g. Sn, In) at low processing temperatures (~ 200 - 300°C). IMC formation in bonding process signifies a very strong mechanical and metallurgical bonding. The resultant IMCs have higher melting temperatures (T_{IMC}) than the processing temperature (~ twice), which aids multiple levels processing on the same wafer without affecting the previously bonded structures. Since Sn is in liquid state at the bonding temperature, therefore surface planarity requirement is not much as that in other bonding techniques. In SLID bonding, initially and a low melting point metal is electroplated over a high melting point metal. Then samples are ramped to intermediate temperature (T_{int}) and then brought in contact and ramped to bonding temperature (T_b). Initially there is some metastable IMC formation (e.g. Cu_6Sn_5 in Cu-Sn couple) at the metal interface. Holding the sample at elevated temperatures for adequate time durations leads to uniform and only layer of thermally stable IMC (e.g. Cu_3Sn in Cu-Sn couple) between the high melting point metal as shown schematically in Fig. 1. IMC growth depends upon thickness and grain size of electroplated metals, as well as the temperature profile applied while bonding. Electroplated metals having fine grains micro-structures results in rapid growth of IMCs due to the increased grain boundaries regions because it provides more nucleation sites and increased grain boundary diffusion [3][4]. Due to the easy availability and low cost, Cu-Sn SLID bonding has attracted a lot of interest. Literature has shown very high potentials for Cu-Sn based SLID bonding [2][5][6]. But a major issue in Cu-Sn SLID bonding is voids formation.

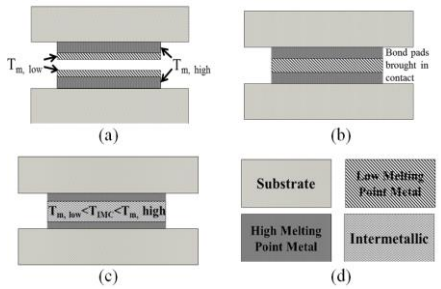

Fig. 1: Schematic of SLID bonding.

*Email: harindra.kannojia39@gmail.com

ISBN: 978-93-80689-28-9

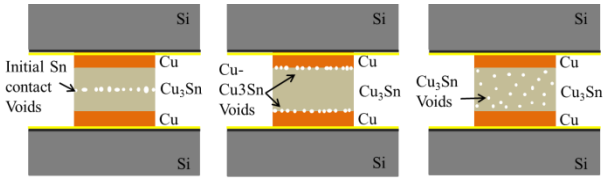

Fig. 2: Voids in Cu-Sn SLID system. (a) Interfacial voids, (b) Kirkendall voids, and (c) Cu-Cu_3Sn voids.

Bond hermeticity, strength and reliability are greatly compromised due to the presence of these intermittent voids which form sporadically at different locations i.e. within IMCs as well as at IMC interfaces. In addition to these detrimental effects, voids reduce the IMC growth [7]. These voids can be attributed to various reasons depending upon their location of occurrence. For example, voids formed in the original contact interface of Sn (Ref. Fig. 2(a)) are ascribed to the unavailability of pure Sn in liquid phase when melting point is reached while bonding and the non-uniform scalloped shaped Cu_6Sn_5 comes into contact from opposite sides to form voids. These voids can be avoided by carefully designing the initial metal thicknesses and bonding temperature profile in order to allow some pure Sn in liquid phase at the melting point [8][9]. Major voids in Cu-Sn SLID stacks include voids in Cu_3Sn IMC and Cu-Cu_3Sn interface as shown in Fig. 2(b-c) schematically. These two voids are predominantly referred to the kirkendall effect but recent research has showed that quality of electroplated Cu critically affects void formation and growth [10]. In this article, we report the void formation in Single Cu-Sn metal stacks annealed at 250 °C, 275 °C and 300 °C for 10, 60 and 150 minutes. Number of voids, void fraction and void sizes are calculated using image processing software. It is observed that voids are generally concentrated in Cu_3Sn IMC and Cu-Cu_3Sn interface. A few voids are observed at Cu_3Sn-Cu_6Sn_5 interface and almost none in Cu_6Sn_5 IMC.

2. EXPERIMENTAL PROCEDURE

Silicon (Si) wafers (2-inch) were used as substrate. Si wafers were initially cleaned using RCA solution. The cleaned Si wafers were oxidized in a dry oxidation furnace to achieve 200 nm silicon oxide layers over entire Si wafer. The oxide layer provides an insulation layer to electrically isolate different bond pad structures. This is followed by sputter deposition of chromium (10 nm) and gold (100 nm) as adhesion/diffusion barrier layer and electroplating seed layer, respectively. Then circular/square shaped bond pads were patterned over the seed layer for selective electrodeposition, using AZ4620 positive-tone photoresist in MJB4 mask aligner. Further, Cu (6 µm) and Sn (3 µm) were sequentially electroplated by pulse electrodeposition having 500 Hz frequency and 50% duty cycle. The peak current density applied while Cu and Sn electroplating was 5 mA/cm^2. Electroplating was performed in using a commercial electrolyte (supplied by Atotech, Germany), with continuous filtration and agitation of electrolyte to achieve uniform and good quality electrodeposits. After electrodeposition, Si wafers were diced into individual dies, which were further annealed at 250 °C, 275 °C and 300 °C for 10, 60 and 150 minutes into a vacuum furnace to avoid oxidation of Cu at elevated temperatures. Samples were not annealed at 300 °C for 150 minutes, since pure Sn was expected (from numerical simulations) to completely transform into Cu_3Sn at 60 minutes of annealing. Annealing temperature was attained in two steps, i.e. firstly the samples were ramped to intermediate temperature (T_{int} = 150 °C) with a ramping rate of 5 °C/min and hold it there for 10 minutes. Then, temperature was ramped to annealing temperature (i.e. 250 °C, 275 °C and 300 °C) with the same ramp rate of 5 °C/min and hold it there for different time durations (10, 60 and 150 minutes). The temperature variation in vacuum furnace was controlled within ±5°C. Once the required annealing time was completed, furnace was switched off and samples were allowed to cool down gradually in the furnace. Dies were then molded into epoxy mold and polished using standard metallographic method to reveal cross-sectional microstructures having subsurface voids formed during annealing. The samples were then observed in scanning electron microscope (SEM) to study void formation and growth at different annealing temperatures and time durations. All micrographs were taken at same magnification i.e. 10,000X for easy comparison. The resolution of the SEM micrograph at this magnification was 0.013 µm pixel^{-1}. Number of voids, void fraction i.e. number of voids per unit length of SEM micrograph and void size were measured using image processing software "ImageJ" to quantify void evolution in Cu-Sn metal stacks. Averaged data were taken from five arbitrary bond pads for each samples annealed at different annealing temperatures and time durations because it is experimentally impossible to infer voiding data from each and every cross-section of bond pads structures. Void growth is completely arbitrary in nature, thus it is fairly assumed that averaged data represents the entire bond pad's behavior

3. RESULT AND DISCUSSION

3.1 Results

Results are compiled to illustrate the voids propensity with respect to annealing temperature and time durations. As an illustration of voids observed in bond pad's cross-sections, SEM micrographs of a bond pad annealed at 250 °C for 10 minutes is shown in Fig. 3. The characterizing voiding parameters i.e. average void size and void fractions are also given for the same micrograph. Non-uniform scalloped shaped Cu_6Sn_5 IMC and comparatively uniform Cu_3Sn IMC can be clearly seen in the SEM micrograph. As a whole observation, significant level of micro voids was observed at Cu-Cu_3Sn interface and within Cu_3Sn IMC. A few voids were also observed at Cu_3Sn-Cu_6Sn_5 interface and within Cu_6Sn_5 IMC. Few to none voids are observed at Cu_6Sn_5-Sn interface. Observed data is presented in terms of two characteristic parameters i.e. variation of void size and of void fractions.

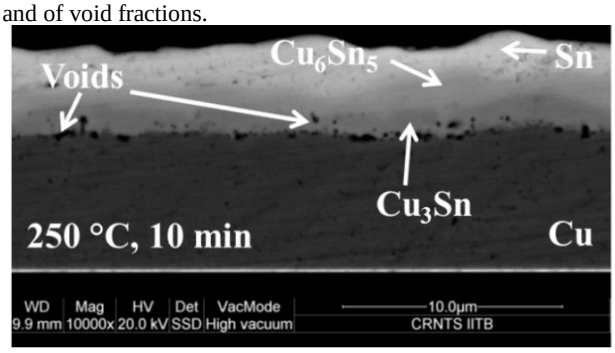

Fig. 3: Voids in Cu-Sn metal stack bond pad with characteristic voiding parameters.

Avg. void size in Cu_3Sn IMC :	0.02 µm^2	Avg. void size at Cu-Cu_3Sn interface :	0.07 µm^2

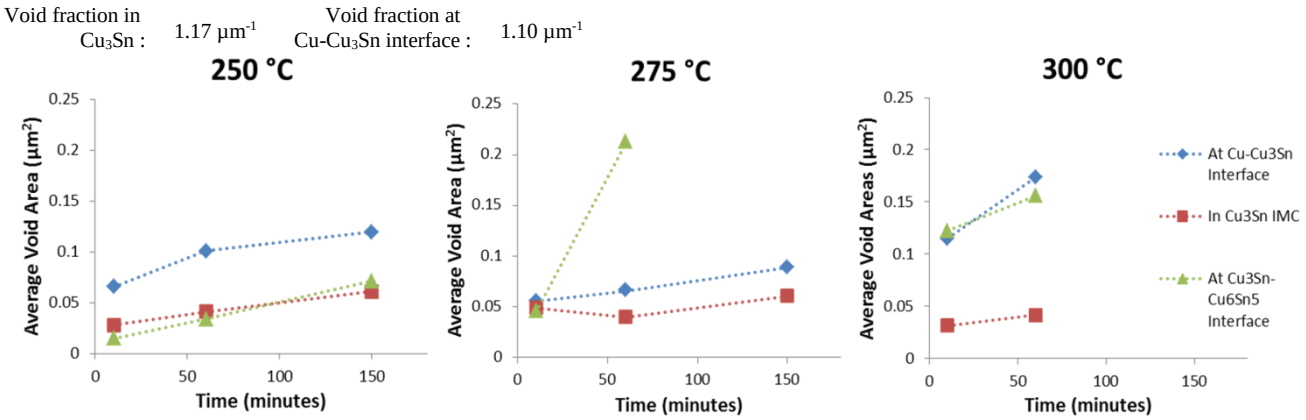

Fig. 4: Variation of average void size as a function of annealing temperature and time durations for (a) 250 °C, (b) 275 °C and (d) 300 °C.

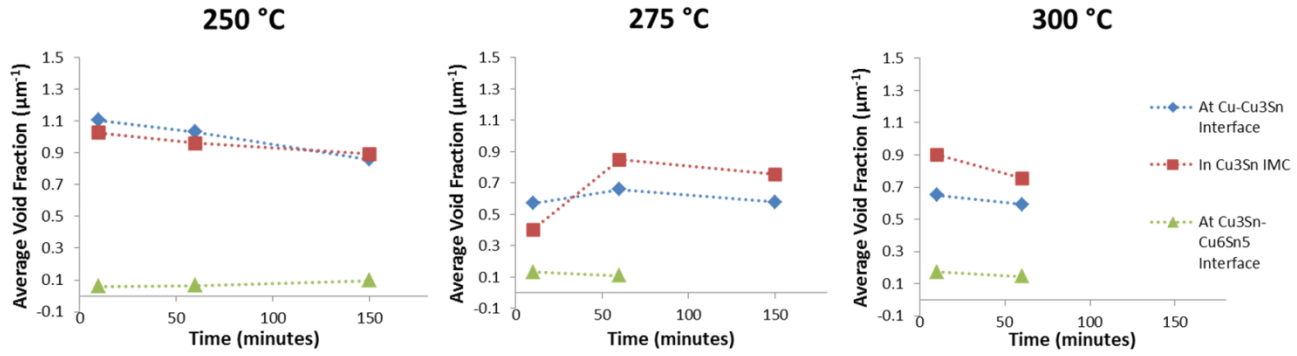

Fig. 5: Variation of void fraction as a function of annealing temperature and time durations for (a) 250 °C, (b) 275 °C and (d) 300 °C.

3.1.1 Average void size

Variation of average void size as a function of annealing temperature and time durations is shown in Fig. 4. From figure it can be seen that, for a given annealing temperature, average void size of all voids, i.e. voids at Cu-Cu_3Sn interface, within Cu_3Sn and Cu_3Sn-Cu_6Sn_5 interface, increases with the increasing annealing time durations. For Cu-Cu_3Sn interface voids, samples annealed at 300 °C showed highest average void sizes. The largest individual void at Cu-Cu_3Sn interface was encountered for sample annealed at 300 °C for 60 minutes, which was 1.44 μm^2, which formed due to the coalescence of several individual smaller voids. For voids within Cu_3Sn IMC, samples annealed at 250 °C showed highest average void size having a largest individual void size of 0.283 μm^2 for 150 minutes of annealing. Samples annealed at 275 °C showed minimum average void sizes for both Cu-Cu_3Sn interface voids and Cu_3Sn voids with smallest individual void size being 0.002 μm^2. Void sizes of Cu_3Sn-Cu_6Sn_5 interface void were minimum for 250 °C samples. No voids were observed at Cu_3Sn-Cu_6Sn_5 interface for samples annealed at 275 °C for 150 which is discussed in next section.

3.1.2 Average void fraction

Variation of void fraction with respect to annealing temperature and time durations is presented in Fig. 5. It is observed that for a given annealing temperature, void fraction decreases with increasing annealing time durations. Samples annealed at 275 °C for 10 minutes showed, out of the trend variation i.e. lower void fraction than the samples annealed at same temperature for higher time durations. The reason for this behavior is not completely clear and requires further investigation. The highest and lowest void fraction for both types of voids (i.e. voids at Cu-Cu_3Sn interface and within Cu_3Sn) were observed in samples annealed at 250 °C for 10 minutes and 300 °C for 60 minutes, respectively. The highest and lowest void fraction were observed to be 1.39μm^{-1} and 0.40 μm^{-1}, respectively. Void fractions of Cu_3Sn-Cu_6Sn_5 interface voids are negligible as seen in Fig. 6.

3.2 Discussion

The reason for increasing void size and decreasing void fraction with increasing annealing time is attributed to coalescence of small sized voids to form larger voids. As annealing proceeds, initially voids tend to nucleate at thermodynamically favored locations like grain boundaries or in the vicinity of impurities, which are incorporated in the metal while electrodeposition. After some time when all the thermodynamic prospective locations are accumulated by voids, the void size tends to increases. This is due to movement and accumulation of diffused vacancies (i.e. due to kirkendall effect) at the pre-existing voids. This is followed by coalescence of smaller nearby voids to form larger voids. The coalescence of voids is clearly observed at Cu-Cu_3Sn interface (ref. Fig. 7). This results in larger voids for longer annealing time duration and at the same time the number of voids decreases too, since they coalesce to form bigger voids. Thus void size shows an increasing trend with increasing annealing time durations and at the same time the void fraction (or

number of voids) shows decreasing trend. The voiding data for samples annealed at 275 °C for 150 minutes, is not presented in the plots, since there were nearly no Cu_3Sn-Cu_6Sn_5 interfaces itself in these samples and even if some small amount of interface was there then there were no voids present, as shown in Fig. 5. The reason for absence of Cu_3Sn-Cu_6Sn_5 interface was unavailability of pure Sn at annealing temperature. Pure Sn flowed away from the bond pad structures while annealing since the temperature was higher than the melting temperature of Sn ($T_{m, Sn}$ = 232 °C).

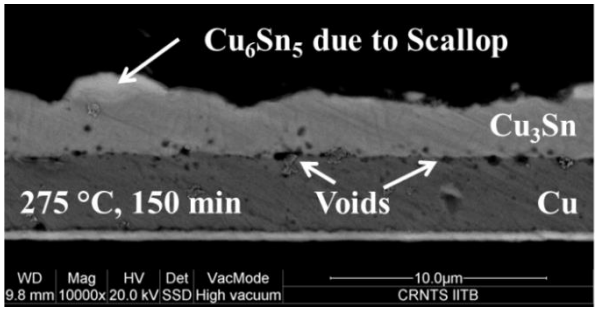

Fig. 6: SEM micrograph of a bond pad annealed at 275 °C for 150 minutes, showing no Cu3Sn-Cu6Sn5 interface voids.

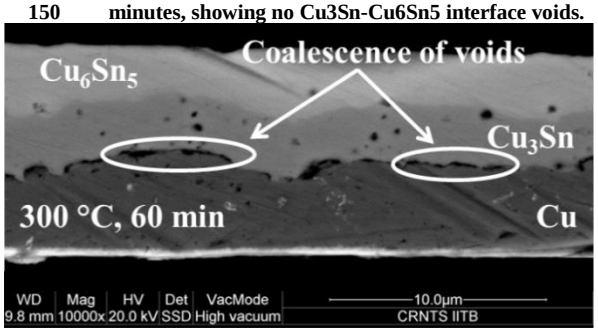

Fig. 7: SEM micrograph of a bond pad annealed at 300 °C for 60 minutes, showing high voiding level at Cu-Cu3Sn interface.

This resulted in reduced Cu_6Sn thickness which, in turn, got completely converted to Cu_3Sn in 150 minutes annealing at 275 °C. Difference in IMC layer thickness can be observed in Fig. 6 and Fig. 7. In Fig. 6, small amount of Cu_6Sn_5 can be seen; this is due to the non-uniform scallops of the Cu_6Sn_5 at some locations, but Cu_3Sn-Cu_6Sn_5 interfaces present do not contain any voids at all. For samples annealed at 300 °C for 60 minutes, the voiding level was observed to be very high at Cu-Cu_3Sn interface that Cu_3Sn IMC layer were separated from the base Cu metal at some locations as shown in Fig. 7. The reason for void formation is attributed mainly to two reasons i.e. first, impurities incorporated into the electrodeposit while electroplating [7] [10] [11], and second, kirkendall effect [12]. Initially Kirkendall effect was suggested to be major cause of voiding in SLID bonded structures but recent studies have shown that electroplating solution and current density influences the void formation and growth.

4. CONCLUSION

Void formation and growth in electroplated Cu-Sn metal stacks at 250 °C, 275 °C and 300 °C has been studied, since high voiding levels affects the strength and reliability of the base Cu metal and formed IMC. It is observed that void size increases and void fraction decreases linearly with annealing time duration for each annealing temperatures. Maximum and minimum void sizes and void fractions were identified depending upon the location of void formation. Minimum voiding levels were observed for sample annealed at 275 °C which makes it a suitable temperature for SLID bonding with low level of voids in the bond structures. Cu-Cu_3Sn interface is found to be very critical due to the higher level of voiding than the other voiding locations i.e. within Cu_3Sn and Cu_3Sn-Cu_6Sn_5 interfaces. When these structures would be used for Cu-Sn-Cu based SLID bonding, optimized bonding temperature will be used to attain hermetic encapsulation with very low to almost no voids in the bonds. This will finally result in improved lifespan, strength and reliability of hermetic encapsulation obtained via Cu-Sn SLID bonding.

Acknowledgment

Industrial Research and Consultancy Centre, IIT-Bombay, is gratefully acknowledged for funding support under 15IRCCSG002 project.

References

[1] M. Esashi, “Wafer level packaging of MEMS,” *J. Micromechanics Microengineering*, **18**, 73001, 2008.

[2] A. Munding, H. Hubner, A. Kaiser, S. Penka, P. Benkart, and E. Kohn, "Cu/Sn Solid–Liquid Interdiffusion Bonding", in *Wafer Level 3-D ICs Process Technology*, C. S. Tan, R. J. Gutmann and L R. Reif, Springer, New York, USA 2008.

[3] Z. Q. Liu, P. J. Shang, A. D. X. Li, and J. K. Shang, “Growth kinetics and microstructural evolution of Cu-Sn intermetallic compounds on different Cu substrates during thermal aging,” in *Int. Conf. on Electron. Pack. Tech. & High Density Pack. (ICEPT-HDP)*, **8**, 569–571, 2009.

[4] H. Liu, K. Wang, K. E. Aasmundtveit, and N. Hoivik, “Intermetallic Compound Formation Mechanisms for Cu-Sn Solid – Liquid Interdiffusion Bonding,” *J. Electron. Mater.*, **41**, 2453–2462, 2012.

[5] H. Huebner, S. Penka, B. Barchmann, M. Eigner, W. Gruber, M. Nobis, S. Janka, G. Kristen, and M. Schneegans, “Microcontacts with sub-30 um pitch for 3D chip-on-chip integration,” *Microelectron. Eng.*, **83**, 2155–2162, 2006.

[6] T. T. Luu, A. N. I. Duan, K. E. Aasmundtveit, and N. Hoivik, “Optimized Cu-Sn Wafer-Level Bonding Using Intermetallic Phase Characterization,” *J. Electron. Mater.*, **42**, 3582–3592, 2013.

[7] J. Y. Kim and J. Yu, “Effects of residual S on Kirkendall void formation at Cu/Sn – 3.5Ag solder joints,” *Acta Mater.*, **56**, 5514–5523, 2008.

[8] N. S. Bosco and F. W. Zok, “Critical interlayer thickness for transient liquid phase bonding in the Cu–Sn system,” *Acta Mater.*, **52**, 2965–2972, 2004.

[9] K. E. Aasmundtveit, T. Luu, K. Wang, and N. Hoivik, “Void Formation in Cu – Sn Solid-Liquid Interdiffusion (SLID) Bonding,” in *Euro. Microelectron. Pack. Conf.*, **9**, 1–6, 2015.

[10] G. Ross, V. Vuorinen, and M. Paulasto-Kröckel, “Void formation and its impact on CuSn intermetallic compound formation,” *J. Alloys Compd.*, **677**, 127–138,

2016.

[11] L. Yin and P. Borgesen, “On the root cause of Kirkendall voiding," in *J. Mater. Res.*, **26**, 455–466, 2011.

[12] A. Paul, “Growth mechanism of phases, Kirkendall voids, marker plane position and indication of the relative mobilities of the species in the interdiffusion zone,” in *J. Mater. Sci. Mater. Electron.*, **22**, 833–837, 2011.